IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S): Sha Li, Shuhua Xiang, Xu Wang

APPLICATION NO.: Not Yet Known

FILING DATE: November 2, 2001

TITLE: Video Processing Control And Scheduling

EXAMINER: Not Yet Known

GROUP ART UNIT: Not Yet Known

ATTY. DKT. NO.: 22682-06281

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AMENDMENT A

SIR:

Prior to examination of this application, please amend the application, as follows.

IN THE SPECIFICATION:

Please delete paragraph **[00112]** on page 45 as originally filed and replace with the following paragraph **[00112]**.

--**[00112]** The video processing system 1400 includes several devices to be

controlled by the scheduler host device 1428. These devices include MEC engine 1432, a compression engine 1436, a memory controller engine 1438, and the external host 1410. MEC engine 1432 includes a motion estimation and motion compensation array 1440, stream buffer 1442 and SRAM 1444. Compression engine 1436 includes a discrete cosine transform (DCT) and inverse DCT (IDCT) module 1446, a quantizer and dequantizer module 1448, a variable length coding (VLC) encoder 1450, and buffers such as block SRAMs 1452, 1454. Additional details of the video compression techniques for video processing system 1400 are disclosed in: (1) U.S. Application No. 09/924,079, entitled "Cell Array and Method of Multiresolution Motion Estimation and Compensation," filed August 7, 2001, by Shuhua Xiang, *et al.,* the subject matter of which is hereby incorporated by reference in its entirety; and (2) U.S. Application No. 09/924,140, entitled "DCT/IDCT With Minimum Multiplication," filed August 7, 2001, by He Ouyang, *et al.*, the subject matter of which is hereby incorporated by reference in its entirety.--

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REMARKS

Applicants are hereby amending the specification to provide updated information related to the U.S. application numbers which have recently been made available from the U.S. Patent and Trademark Office for the pending U.S. applications incorporated by reference. Consequently, Applicants respectfully request entry of the amendment of the specification in the instant application.

Applicants believe that this application is in condition for allowance, and

therefore an early Notice of Allowance is respectfully requested.

Respectfully submitted,

SHA LI, SHUHUA XIANG, XU WANG

Dated: November 2, 2001

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

[00112] The video processing system 1400 includes several devices to be controlled by the scheduler host device 1428. These devices include MEC engine 1432, a compression engine 1436, a memory controller engine 1438, and the external host 1410. MEC engine 1432 includes a motion estimation and motion compensation array 1440, stream buffer 1442 and SRAM 1444. Compression engine 1436 includes a discrete cosine transform (DCT) and inverse DCT (IDCT) module 1446, a quantizer and dequantizer module 1448, a variable length coding (VLC) encoder 1450, and buffers such as block SRAMs 1452, 1454. Additional details of the video compression techniques for video processing system 1400 are disclosed in: (1) U.S. Application No.[, Attorney Docket 22682-6188] 09/924,079, entitled "Cell Array and Method of Multiresolution Motion Estimation and Compensation," filed August [3] 7, 2001, by Shuhua Xiang, *et al.*, the subject matter of which is hereby incorporated by reference in its entirety; and (2) U.S. Application No.[, Attorney Docket 22682-6189] 09/924,140, entitled "DCT/IDCT With Minimum Multiplication," filed August [3] 7, 2001, by He Ouyang, *et al.*, the subject matter of which is hereby incorporated by reference in its entirety.

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